PATENT CLAIMS:

1. A method of making a contact between a first layer (5;25;35;45;55;65;75a,b) and a layer (1;21;31;41;71;57;67;77) bounding or adjacent the first layer, characterized in that:

a passivation element is deposited or incorporated in or on the first layer (25;55) and/or the adjoining layer (1;21;31;41) or in a starting component for these layers (34;54;64;68;71) by ion implantation, and

the passivation element by means of a thermal treatment is enriched in at least one interface (6a,b;26a,b;46a,b;66a,b; 76a,b) between the first layer and the adjoining layer.

2. A method of making a contact between a first layer (5;25;35;45;55;65;75a,b) and a layer (1;21;31;41;71;57;67;77) bounding or adjacent the first layer, characterized in that:

a passivation element is applied or introduced into or on the adjacent layer (1;21;31;41) by means of ion implantation or deposition and/or in the silicide (25;55) or in its metallic (34;54;64) and/or silicon containing (68;71) component, and

by means of a thermal treatment for the passivation

element is enriched in at least one interface (6a,b;26a,b;36a,b; 46a,b;66a,b;76a,b) of the silicide to the adjoining layer.

3. The method according to claims 1 or 2 characterized in that as the first layer a metal silicide, a semiconductor silicide and a metal germanide or a metal is selected.

4. The method according to one of the preceding claims characterized in that as the adjoining layer a semiconductor layer or a dielectric is selected.

5. The method according to one of the preceding patent claims characterized in that silicon is chosen as the material for the adjoining layer.

6. The method according to one of the preceding claims characterized in that the passivation element is implanted or deposited before or after the production of the silicide or germanide.

7. The method according to one of the preceding claims characterized by at least one thermal treatment to produce the silicide or germanide.

8. The method according to one of the preceding claims characterized in that by a thermal treatment the first layer is formed and the passivation of the interface or interfaces to the adjoining layer is effected.

9. The method according to one of the preceding claims characterized in that for the enrichment of the interface with the passivation element between the first layer and the adjoining layer is effected during a solidization.

10. The method according to one of the preceding patent claims characterized by the choice of a chalcogen as the passivation element.

11. The method according to one of the preceding claims characterized by the choice of selenium, sulfur or tellurium as the chalcogen.

12. The method according to one of the preceding patent claims characterized in that the passivation element is implanted with a dose of 10^{12} to 10^{16} cm^{-2}, especially 10^{14} to 10^{15} cm^{-2}.

13. The method according to one of the preceding claims characterized in that the metal component of the metal silicide or metal germanide is selected from the group of cobalt, nickel, titanium, tungsten and/or molybdenum.

14. The method according to one of the preceding claims characterized in that the silicon component of the silicide as the first layer is comprised of polysilicon or amorphous silicon.

15. The method according to one of the preceding claims characterized by the choice of β-$FeSi_2$, Ru_2Si_3, $MnSi_x$ or $CrSi_2$ as a semiconductor silicide.

16. The method according to one of the preceding patent claims characterized in that a mask is arranged on the adjoining layer.

17. An electronic component comprised of at least one passivated metal-semiconductor or metal-insulator contact made in accordance with one of the preceding patent claims.

18. A Schottky barrier MOSFET with an adjustable, especially negative Schottky barrier as the source and/or drain contact of an electronic component according to claim 17.

19. A Schottky barrier MOSFET according to claim 18 characterized in that the contact has a silicon thickness smaller than 30 nm arranged on an ultra thin SOI substrate.

20. A MOSFET with a gate contact adjusted by means of passivation as an electronic component according to one of claims 17 to 19.

21. A spin transistor as the electronic component according to claim 17 characterized in that a semiconductor silicide is selected as the first layer with Mn or Fe or Co doping for the formation of magnetic source and drain contacts.